EXHIBIT B

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HTC CORPORATION and
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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION and HTC AMERICA, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOTIC SCIENTIFIC CORPORATION and ALLIACENSE LIMITED,

Defendants.

Case No. 5:08-CV-00882 PSG

(Related to Case Nos. C-08-05398 PSG and C-08-00877 PSG)

EXPERT REPORT OF DAVID MAY ON THE INVALIDITY OF U.S. PATENT NO. 5,530,890

jumps to the return address. The AJW instruction is used by a called procedure to allocate and deallocate space for items in the WPTR stack. The items in the WPTR stack are accessed relative to the stack pointer (WPTR) by the load local (LDL) and store local (STL) instructions, as described in section 5.2. [*See* HTCTP 10218095].

VIII. CLAIM CONSTRUCTION

111. I have been informed that the claim constructions as set forth by the judge control the scope of the claims. In performing my analysis, I applied the Court's claim construction orders dated June 12, 2012 and December 4, 2012.

112. The Court provided the following constructions on June 12, 2012 relating to the '890 patent:

Claim Term	Court's Construction
"push down stack connected to said arithmetic logic unit"	*A last-in-first-out data storage element connected to the arithmetic logic unit.*
"instruction register"	*Plain and ordinary meaning*
"separate direct memory access central processing unit"	*A central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit.*
"ring oscillator"	*Requested supplemental briefing*
"clocking said central processing unit"	*Providing a timing signal to said central processing unit.*
"as a function of parameter variation"	*Plain and ordinary meaning*
"providing an entire variable speed clock disposed upon said integrated circuit substrate"	*Providing a variable speed clock that is located entirely on the same semiconductor substrate as the central processing unit.*
"wherein said central processing unit operates asynchronously to said input/output interface"	*The timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them.*

113. On December 4, 2012, the Court issued its second claim construction order:

Claim Term	Court's Construction
"instruction register"	*Register that receives and holds one or more instructions for supplying to circuits that interpret the instructions*
"ring oscillator"	*an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment*
"separate DMA CPU"	*a central processing unit that accesses memory and that fetches and executes instructions directly and separately of the main central processing unit*

114. I also understand that the parties agreed to the following claim constructions regarding the '890 patent which I have used in my analysis:

Claim Term	Agreed Construction
mode register	*register that stores mode bits*
return stack pointer	*A storage element in the main central processing unit, separate and distinct from the stack pointer, that stores a value representing a location in the return push down stack*
loop counter	*A counter circuit in the main CPU that stores a variable value representing a remaining number of times a particular instruction or group of instructions is to be executed by the main CPU*
a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate	*Capable of operating at different frequencies as a function of changes in at least one fabrication or operational parameter associated with the integrated circuit substrate*
oscillator	*A circuit capable of maintaining an alternating output*
on-chip input/output interface	*A circuit having logic for input/output communications, where that circuit is located on the same semiconductor*

	substrate as the CPU
integrated circuit	*A miniature circuit on a single semiconductor substrate*
Microprocessor	*An electronic circuit that interprets and executes programmed instructions*

IX. THE PRIOR ART DISLCOSES EACH LIMITATION OF THE ASSERTED CLAIMS

A. The '890 Patent

1. Common Opinions

115. It is my opinion that the following references anticipate or render obvious each and every element of the asserted claims of the '890 patent, thus rendering these claims invalid. To support this opinion, I have attached invalidity claim charts as Exhibits G and H to this report, which provides a detailed analysis of each element. To the extent TPL argues that an element is not explicitly or inherently disclosed by my report, it is my opinion that the given disclosure is so close to the claimed elements that any differences would have been obvious to one of ordinary skill in the art.

2. Transputer Architecture

116. The Transputer processor was developed in the 1980s by INMOS and was a microprocessor designed for the construction of multiprocessor systems. The first products were launched in 1984.

117. The Transputer is described by many references that were published in the 1980s. For the sake of conciseness, I have relied on the following three references to describe the overall structure and functionality of the Transputer as it was publically known prior to August 3, 1989 (hereinafter referred to generally as "Transputer Architecture"):

The Transputer Architecture	
1	The Transputer Reference Manual ("Transputer Reference Manual") published in the United States in 1988 by Prentice Hall International and discloses pioneering microprocessor architecture of the 1980s, featuring integrated memory and serial communication links, intended for parallel computing. It was designed and produced by INMOS, a semiconductor

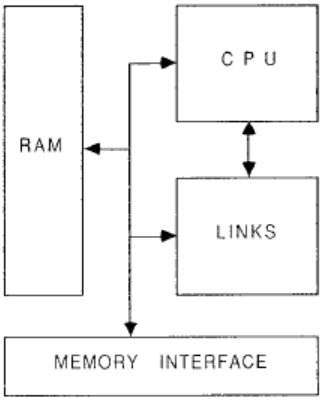
	company based in Bristol, England. (*See* HTCTP00111842 – HTCTP0112208)
2	The IMS T414 Transputer, Product Description published by INMOS in September 1985 (*See* HTCTP10218031 – HTCTP10218046)
3	Transputer Instruction Set: a compiler writer's guide published by Prentice Hall in 1988 (*See* HTCTP10218078 - HTCTP10218250)

118. I have based my invalidity opinions below on TPL's broad reading of the '890 patent as found in its infringement contentions. It is my opinion that TPL appears to utilize overly broad constructions of various limitations of the asserted claims of the '890 patent in an effort to assemble an infringement claim where none exists and to accuse products that do not practice the claims. My analysis takes into account TPL's overly broad construction of the claim limitations. Any assertion that a particular limitation is disclosed by a prior art reference or references may be based on TPL's apparent constructions and is not intended to be, and is not, an admission that such constructions are supportable or correct.

119. As I will explain below, it is my opinion that the Transputer discloses, or renders obvious (alone or in combination with other references), all the limitations of the asserted claims of the '890 patent under the Court's claim constructions. It is also my opinion that the Transputer discloses, or renders obvious (alone or in combination with other references), all the limitations of the asserted claims of the '890 patent under all of TPL's claim construction positions contained within its claim construction briefing. It is also my opinion that the Transputer discloses, or renders obvious (alone or in combination with other references), all the limitations of the asserted claims of the '890 patent under all of HTC's claim construction positions contained within its claim construction briefing.

120. To the extent that any of the prior art discloses the same or similar functionality, feature, or features of any of the accused products that is found to practice any limitation of the asserted claims of the '890 patent, then I understand that the prior art reference discloses or renders obvious the limitation.

121. In my analysis, I have also cited other references to provide context or further



IMS T414

[HTCTP0111889].

(c) and a separate direct memory access central processing unit in a single integrated circuit comprising said microprocessor

125. The Court has construed "separate direct memory access central processing unit" as "a central processing unit that accesses memory and that fetches and executes instructions directly and separately of the main central processing unit." One skilled in the art, however, will understand that a "separate direct memory access central processing unit" is dedicated to performing "direct memory access" operations. Otherwise, the term "direct memory access," or 'DMA,' in this limitation would be superfluous. This is confirmed in Figure 5 (shown on the right) of the '890 patent, which shows a basic DMA architecture, compared with the complex main CPU architecture shown in Figure 2.

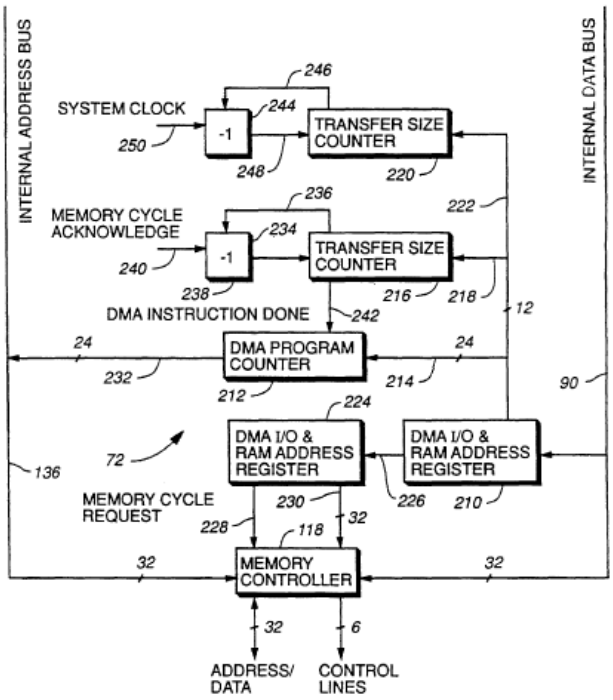


FIG._5

126. Under the Court's construction, the Transputer Architecture discloses or renders obvious this limitation.

127. For example, the Transputer Reference Manual discloses the use of multiple Transputers in a network which communicate with each other over point to point communication links. As shown below, every Transputer has four links and each link is able to perform DMA transfers, via a controller, in both directions. Each of the Transputers has the ability to access memory and fetch and execute instructions.

> A transputer can be used in a single processor system or in networks to build high performance concurrent systems. A network of transputers and peripheral controllers is easily constructed using point-to-point communication.
>
> [HTCTP0111864]

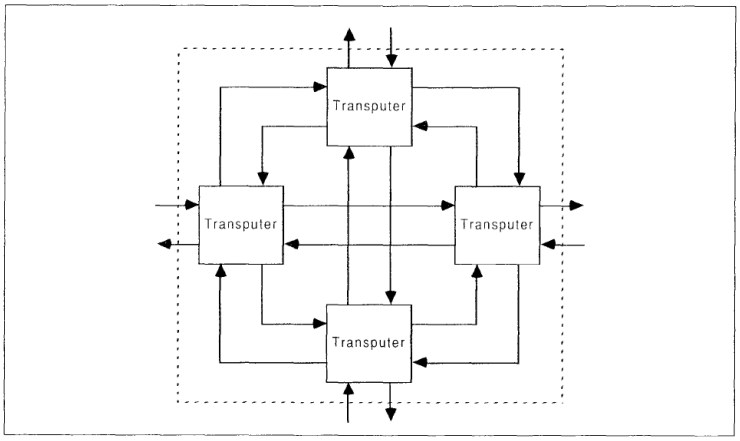


Figure 1.3: A node of four transputers

> [HTCTP0111865]

128. The Transputer Reference Manual goes on to explain that multiple transputers can be constructed on a single chip and that each transputer contains memory:

> A system, perhaps constructed on a single chip, can be built from a combination of software processes, preprogrammed transputers and hardware processes. Such a system can, itself, be regarded as a component in a larger system.
>
> [HTCTP0111866]
>
> In a computer, almost every operation that the processor performs involves the use of memory. For this reason a transputer includes

both processor and memory in the same integrated circuit device.

[HTCTP0111887]

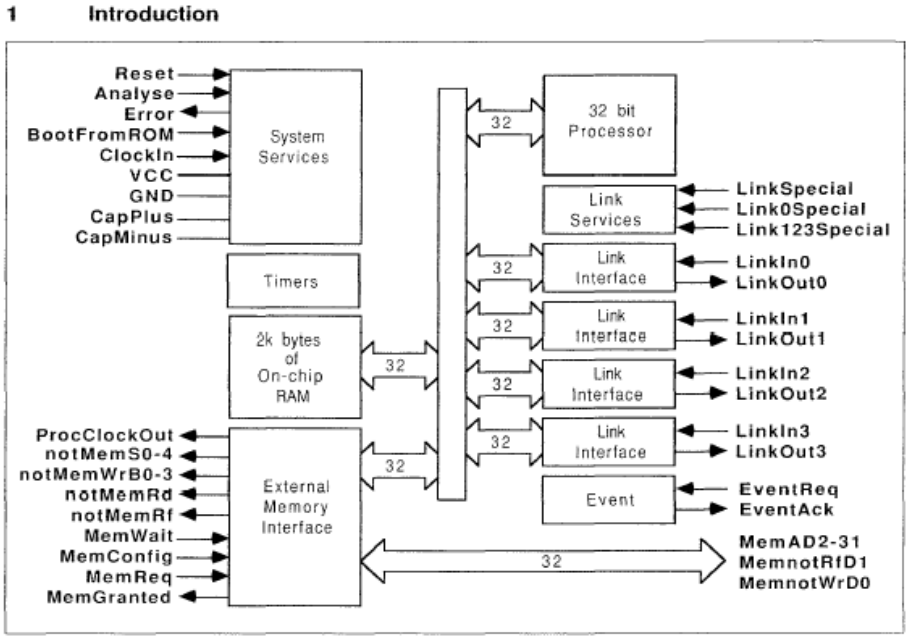


Figure 1.1: IMS T414 block diagram

[HTCTP0111969]

129. Furthermore, it would have been obvious to replace one or more of the Transputer's DMA link controllers with a programmable DMA CPU. The motivation would be to provide more flexible control over the I/O interface.

130. Dual processor systems were well known as early as the mid 1980s to handle the additional complexity of computer interfaces. U.S. Patent No. 4,679,166 (the "'166 patent"), which claims priority to a Jan 17, 1983 application, discloses a dual processor system which allowed additional functionality such as video processing.

> A dual processor system in which one processor is dedicated to input/output tasks while the other is dedicated to high level language tasks when operating as a 16-bit machine.

[HTCTP10218691, the '166 patent, Abstract]

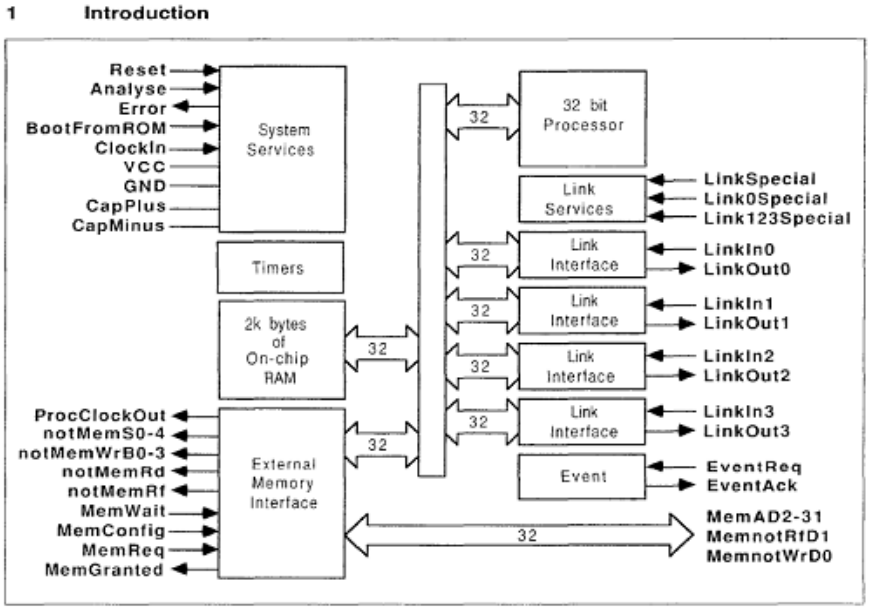


Figure 1.1: IMS T414 block diagram

(HTCTP0111969)

The instruction representation gives a more compact representation of high level language programs than more conventional instruction sets. Since a program requires less store to represent it, less of the memory bandwidth is taken up with fetching instructions. Furthermore, as memory is word accessed the processor will receive four instructions for every fetch.

(HTCTP0111912)

(4) Claim 17

(a) The microprocessor of claim 11 additionally comprising A ring oscillator variable speed system clock connected to said main central processing unit and said ring oscillator variable speed system clock being provided in a single integrated circuit.

192. The Court has construed the claim term "ring oscillator" as "an oscillator having multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment."

193. Under the Court's construction, and HTC's construction, it would have been obvious to one skilled in the art at the time of the invention to attempt to combine the Transputer with a "ring oscillator variable speed system clock," to avoid the need of constructing an on-chip

Phase Locked Loop. This type of system was disclosed in Introduction to VLSI Systems by Mead & Conway. [*See* HTCTP10219186 - HTCTP10219618]. The motivation would have been to enable high speed internal operation together with low-speed external interfaces.

194. The Mead and Conway text states:

> Process variation in integrated circuit fabrication does not allow accurate resonant networks to be fabricated by usual means, but it is perfectly feasible, indeed essential for self-contained VLSI systems, to generate clock signals on the chip.
>
> [HTCTP10219451]
>
> The easiest way to build these timers is as chains of inverters. The propagation delay time of such a chain will of course vary with tau, according to the way in which the fabrication process, aging, temperature, and power voltage affect tau.
>
> [HTCTP10219452]
>
> However, these variations only make the inverter chain a better model of the system being clocked than a fixed timer would be, since on the same piece of silicon these variable factors are nearly the same for the clock and for the system.
>
> [HTCTP10219452]
>
> Clocks that employ these delays as timers are all elaborations of the *ring oscillator* circuit shown in Fig. 7.9(a). Rings of an odd number of inversions have no stable condition and will oscillate with a period that is some odd submultiple of the delay time twice around the ring.
>
> [HTCTP10219453]

195. Additionally, U.S. Patent No. 4,691,124 ("Ledzius") discloses a "ring oscillator variable speed system clock" based on the Court's construction of "ring oscillator." Ledzius describes a variable frequency oscillator whose oscillation frequency is intended to match the timing of on-chip logic circuits under varying environmental conditions. An odd number of inversions arranged in a loop can be identified in this variable frequency oscillator whose speed depends on environmental parameters. It can be stopped and started to allow synchronization with an external interface. Among other things, the speed of the clock is determined by the delay

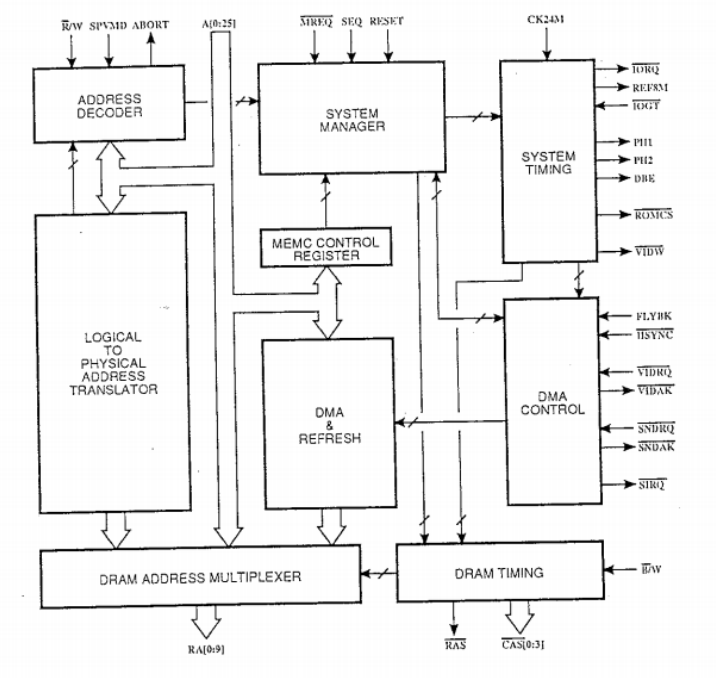
(c) and a separate direct memory access central processing unit in a single integrated circuit comprising said microprocessor

207. The Court has construed "separate direct memory access central processing unit" as "a central processing unit that accesses memory and that fetches and executes instructions directly and separately of the main central processing unit." As discussed above, however, one skilled in the art will understand that a "separate direct memory access central processing unit" is dedicated to performing "direct memory access" operations. Otherwise, the term "direct memory access," or 'DMA,' in this limitation would be superfluous. This is confirmed in Figure 5 of the '890 patent, which shows a basic DMA architecture, compared with the complex main CPU architecture shown in Figure 2.

208. Under the Court's construction, the ARM Architecture discloses or renders obvious this limitation. For example, the 1987 ARM Datasheet discloses the use of co-processor capability which requires addition of "further logic" to an "integrated memory controller":

> MEMC (VTI part number VL86C 110) is an integrated memory controller for ARM which incorporates an address translation system and generates all the critical system timing signals.… If Co-Processor capability is required, further logic must be added to modify the behaviour of MEMC.
>
> [HTCTP10217849, Datasheet at 52]

209. The MEMC was a separate chip also developed in the mid 1980s that controlled DMA operations. The chip was another ACORN product like the ARM processor and was produced at about the same time. The MEMC Datasheet (also published in the 1980s), shown below, discloses a DMA controller that allowed for the addition of further logic to provide co-processor capability. [*See* HTCTP10218759 – HTCTP10218836].



[*See* HTCTP10218759 – HTCTP10218836]

X. THE '890 PATENT IS INVALID

A. Lack of Enablement and/or Written Description under 35 U.S.C. § 112(1)

249. Claim 13 are invalid for lack of enablement and written description. In particular, the specification does not provide a sufficient disclosure of how to make the claimed "ring oscillator variable speed system clock." There is no explanation as to how an entire CPU can be constructed in such a way that its circuits will vary in the same way as a simple chain of inverters. CPUs normally include a variety of different circuit structures and wires of differing lengths. Without a novel approach to the construction of a CPU, it would be impossible to use the proposed form of oscillator. This is not described in the disclosure. The situation becomes more complex when a CPU and a RAM or DRAM are combined on the same chip. RAMs and DRAMs use circuit structures optimised so as to pack as much information as possible into the smallest space. DRAMs use different steps in the manufacturing process from those used in processors. The disclosure does not point out these problems and offers no way to overcome them.

250. Claim 11 is invalid for lack of enablement and written description. In particular,

the specification does not provide a sufficient disclosure of how to make the claimed "stack pointer pointing into said first push down stack." The operation of the stack pointers is not explained in the specification. For example, the diagram in Figure 21 (shown below) shows three parts of a stack.

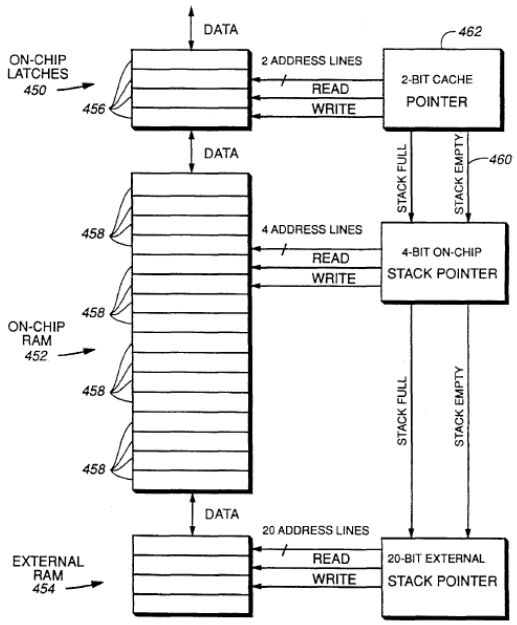


FIG._21

251. When four items have been pushed onto the stack 450, it is unclear what happens to the items and the pointer when a fifth item is pushed. It is not clear whether the registers 450 are intended to include the top item and next item, or how the ALU is connected. It is also unclear with respect to registers 452 what happens when a seventeenth item is pushed onto the stack. The disclosure therefore does not adequately disclose claim 11's requiring a pointer 'pointing into a stack.'

252. Each and every claim of the '890 patent is invalid because the specification does not enable one skilled in the art to practice the claimed invention without undue experimentation. In particular, the specification fails to sufficiently describe an essential element of each claim: "a separate direct memory access central processing unit."

253. Nowhere in the specification is the instruction set of the DMA CPU provided. Nor does the '890 specification provide any description of how the main CPU and the separate DMA

CPU interact, such as how the main CPU indicates to the DMA CPU what input-output operations to perform.

254. For example, the description of the DMA CPU is very brief, consisting of Col 8 lines 1-24 and Figure 5. This gives no information about how instructions are fetched and issued, or what the instruction format(s) are. It gives no definition of the instructions to be provided. Without this, it is impossible to understand what exactly the capabilities of the DMA CPU are. There is certainly not enough information to build one. Note that for the CPU, there is a fairly extensive description of the instruction fetch and issue, and of the instruction set (Cols 22-32).

255. The description of the DMA CPU does not describe its clock, or the relationship of its clock to the CPU clock or the relationship of its clock to the input-output interface. It is also unknown whether the DMA CPU has its own "variable speed clock." It is also unknown whether the DMA CPU exchanges coupling control, address and data signals with the input-output interface.

XI. OBJECTIVE INDICIA OF NON-OBVIOUSNESS

256. I stated my understanding above that in determining obviousness, objective indicia (also known as secondary considerations) must also be considered. Examples of objective indicia are commercial success, long felt but unresolved needs, failure of others, and licensing of the invention.

257. I am not aware of any evidence of objective indicia that would preclude a finding of obviousness. For example, I have seen no evidence that a long-felt yet unresolved need existed for the claimed invention at the time of the initial filing or that the invention achieved unexpected results. It is my understanding that the patented-technology was a commercial failure. Various prior art references, including those discussed in this report, disclose every element of all the asserted claims. Any need for the claimed invention had already been met and was not unresolved—it had already been addressed prior to August 3, 1989. Any results achieved by the invention, were entirely predictable, expected, and in line with accepted wisdom.

258. In addition, I have examined TPL's response to HTC's Interrogatory No. 11 served on February 8, 2013. [Exhibit F]. And I am aware that TPL has licensed the '890 patent

to several former defendants in this case. While I am not a licensing expert, the mere existence of settlement agreements involving the '890 patent does not overcome my conclusions of obviousness.

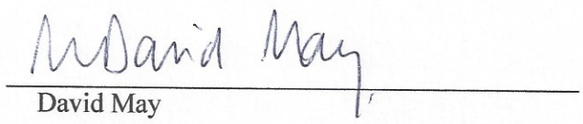
259. Should TPL identify any other specific objective indicia of non-obviousness, I may supplement my report to address such evidence.

XII. CONCLUSION

260. I will be prepared to testify in deposition and at trial as to the specific details of this report. This expert report is based upon the information available to me at the present time. I reserve the right to supplement or amend this report in the event that new information is made available to me.

261. I declare under penalty of perjury under the laws of the United States of America that all statements and affirmations made herein of my own knowledge are true and correct, and all statements made on information and belief are believed to be true and correct.

Dated: June 4, 2013



David May